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Self-Aligned Complementary Bipolar Technology for Low-Power Dissipation and Ultra-High-Speed LSI's

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***Abstract*— Fully symmetrical complementary bipolar transistors for low power-dissipation and ultra-high-speed LSI's have been integrated in the same chip using a 0.3-μm SPOTEC process. Reducing the surface concentration of the boron by oxidation at the surface of the boron diffusion layer suppressed the upward diffusion of boron from the subcollector of the *pnp* transistor during epitaxial growth. This enabled thin epitaxial layer growth for both *npn* and *pnp* transistors simultaneously. Cutoff frequencies of 30 and 32 GHz were obtained in *npn* and *pnp* transistors, respectively. Simulated results showed that the power dissipation is reduced to 1/5 in a complementary active pull-down circuit compared with an ECL circuit.**

I. Introduction

IT is necessary to raise current drivability in transistors to achieve higher-speed and larger-integrated LSI's. As bipolar devices have the advantage of obtaining higher-current drivability than field-effect transistors, they are widely used in high-speed LSI's. Power dissipation in bipolar LSI's, however, is increasing as high-speed performance is improved. It is approaching the cooling limit. Reducing the power dissipation is strongly demanded for future ultra-high-speed LSI's.

One of the effective methods to reduce the power dissipation is to cut off the stand-by current which flows constantly both in the current switches and the emitter followers and keeps the drivability. Active pull-down (APD) circuits which require a pull-down transistor in the emitter follower part can cut off the constant current in the emitter follower part [1]–[5]. The preparation delay is longer in the active pull-down circuit than that in a conventional circuit such as ECL or NTL when the loading at the output node is very small, because the pull-down transistor itself becomes the load for the current switch. On the other hand, the delay time at the same power dissipation becomes smaller when the load at the output node is large, which is possible in actual LSI's. However, these conventional APD circuits easily suffer from the cross-talk and hazard noise, lack logic versatility and have complexity in design [6]–[8].

A capacitor-coupled complementary emitter-follower circuit has been proposed to solve these problems [6]. This circuit requires high-speed *pnp* transistors on the same chip with *npn* transistors in the emitter follower part. Power dissipation is expected to be reduced to a half or less for this circuit compared with a conventional ECL gate.

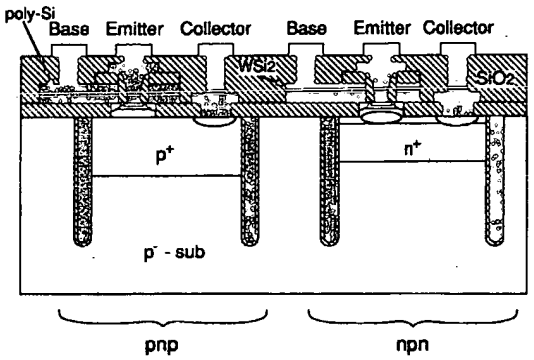

Fig. 1. Schematic cross section of complementary bipolar transistors.

There have been reports of vertical *pnps* with a self-aligned structure having a cutoff frequency of over 30 GHz for high-speed complementary circuits [9]–[13]. Since these reports, interest has been shown in the integration of both high performance *npn* and *pnp* transistors [14]–[15]. Matching of performance between *npn* and *pnp* transistors is also important because the circuit performance is limited by the device with inferior performance. High-performance complementary bipolar devices are also useful for analog LSI's with high frequency cellular or optical communication systems. A *pnp* load amplifier will be required in future high frequency analog circuits because breakdown voltages become small in compensation for high cutoff frequencies. This paper reports the integration of *npn/pnp* self-aligned bipolar transistors with fully symmetrical performance.

II. Device Structure and Process Technology

A. Device Structure

Ultra-high-speed large-scale gate arrays require high-performance bipolar transistors which have small parasitic resistance, high cutoff frequency, and small base resistance. A self-aligned structure with double poly-silicon layers is necessary to obtain such performance. Furthermore, a very small transistor area is necessary to achieve high packing density [16]. A vertical structure in both transistors is suitable for obtaining high cutoff frequency because controllability for shallow junction formation in a vertical structure is superior to that in a lateral structure.

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SPOTEC (Sidewall Polycide Technology) has been proposed to obtain both high-performance and small-area transistors [17]. The complementary bipolar transistors were fabricated by the 0.3-μm-SPOTEC process. Fig. 1 shows the cross section of the complementary SPOTEC transistors. A tungstensilicide film was formed on the surface and sidewall of the polysilicon base electrode of the *npn* transistor. The silicide film was not formed for the *pnp* transistor because the sheet resistance of the *n*-type polysilicon which forms the base electrode of the *pnp* transistor is lower than that of the *p*-type polysilicon for the *npn* transistor. The sheet resistance of the base electrode was 20 $\Omega/\square$ with silicide for an *npn* and 50 $\Omega/\square$ for a *pnp* transistor. The SPOTEC process has a self-aligned isolation, base contact area, emitter, and base electrode with one photo mask. So, this structure achieves small parasitic capacitance, small base resistance, and small transistor area. Both *npn* and *pnp* transistors have the same structure except that the dopant profiles are symmetrical. *pnp* transistors were not isolated from the substrate because the substrate and the collector of the *pnp* transistor in our complementary circuit (Fig. 5) are biased at the same voltage. It is easy, however, to isolate the *pnp* transistor by using bonded SOI wafers for other types of complementary circuits, Darlington type complementary circuit [6], complementary push-pull ECL [5], and *pnp* load amplifier, for example, as shown in Ref. [14]. SOI structure is also very effective in reducing substrate capacitance.

B. Process Technology

The main difficulty in achieving high-performance *pnp* transistors is making an epitaxial layer having the same thickness as in *npn* transistors, because boron in the subcollector of the *pnp* transistor diffuses faster during the epitaxial growth and heat treatment than antimony in the subcollector of *npn* transistors. In our method, upward diffusion of boron was suppressed by reducing the concentration of boron at the surface by thermal oxidation. A thin epitaxial layer of only 0.5 μm was achieved for both *pnp* and *npn* transistors through this treatment. Upward diffusion in this process becomes 0.1 μm smaller than that without this treatment.

The fabrication process flow for complementary bipolar transistors is shown in Fig. 2. The *n*- and *p*-type buried layers were formed by solid phase diffusion of antimony and boron in the *p*-type substrate. Antimony diffusion was conducted before boron diffusion to avoid excess boron diffusion during antimony diffusion.

A 0.5-μm *n*-type epitaxial layer was then grown. Two-step boron implantation (150 keV, 1×10^{13} cm^{-2}; 50 keV, 3×10^{11} cm^{-2}) was then conducted to compensate for the *n*-type epitaxial layer in the *pnp* transistor. 3-μm-deep and 0.7-μm-wide groove was formed with low-temperature ion etching. The groove was certainly *U*-shaped since the bottom of the trench was rounded by this etching. The *U*-groove was filled with CVD-SiO_2 and poly-silicon. The collector (P^+, 120 keV, 5×10^{12} cm^{-2}) and base (BF_2^+, 25 keV, 1.5×10^{14} cm^{-2}) implantation for *npn* transistors and base (As^+, 60 keV, 5×10^{13} cm^{-2}) implantation for *pnp* transistors through 20-nm-thick oxide film were followed by activation annealing at 900°C for 10 min in a furnace. BF_2^+ was then implanted in the *pnp* emitter poly-silicon (25 keV, 1×10^{16} cm^{-2}). After the activation annealing at 950°C, 30 sec with rapid thermal annealing (RTA), arsenic was implanted for the *npn* emitter (60 keV, 2×10^{16} cm^{-2}) and RTA of 950°C, 20 sec was then conducted. Vertical structure design described above is compatible to any other structures.

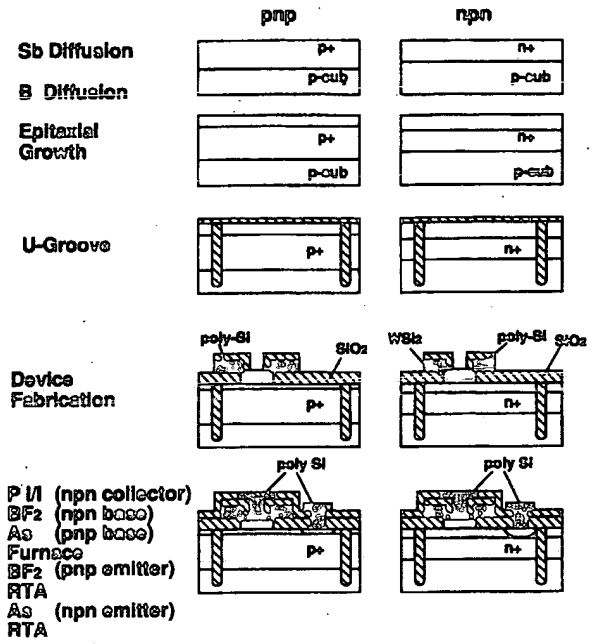

Fig. 2. Fabrication process flow for complementary bipolar transistors.

This process requires three additional masks for the collector diffusion and the base and emitter implantation compared with the fabrication of *npn* transistors. Therefore, the complexity of the process was not significantly increased. Exactly the same structures were formed except that the dopants are symmetrical.

Fig. 3 shows the dopant profiles obtained with spreading resistance profiler, SRP2, by Solid State Measurement Inc. Dopant concentrations in the emitter poly-Si are ambiguous because mobility of the carriers in the poly-Si is not installed in the SRP system. Very thin bases of 40 nm for the *npn* transistor and 30 nm for the *pnp* transistor were achieved.

III. Electrical Results

A. Device Characteristics

Current gains (h_{FE}) of 120 and 80 in the *npn* and *pnp* transistors, and breakdown voltage between the collector and the emitter (BV_{CEO}) of 3 V in both transistors were obtained for emitter size of 0.4×1.6 μm^2. The maximum cutoff frequency of 25/25.5 GHz for $V_{CE} = 1$ V and 30/32 GHz for $V_{CE} = 3$ V in *npn/pnp* transistors for emitter size of 0.4 ×